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D. Remarks

Rejection of Claims 1-20 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,812,414 (*Butts et al.*).

The rejection of claims 1-14 will first be addressed.

The invention of claim 1 is directed to an integrated circuit device that includes a programmable portion comprising a plurality of circuits configurable by a user of the integrated circuit device. The integrated circuit device also includes at least one communication portion comprising at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference. Because the reference, *Butts et al.*, does not show all elements of claim 1, this ground of rejection is traversed.

To best address this ground for rejection, Applicants believe a brief review of the reference *Butts et al.* will be helpful. *Butts et al.* is directed to a hardware emulator that can include multiple electrically reconfigurable gate array chips that can be interconnected by reconfigurable interconnect chips. In realizing various designs, the invention of *Butts et al.* "converts" a netlist representation of a design into a configuration bit pattern file. The bit pattern file is then used to program the gate array device. It is emphasized that this conversion is not performed by any integrated circuit of the system, but by a software tool provided by a vendor:

> [M]anufacturers of ERCGA devices commonly offer netlist conversion **software tools**, which convert logic specifications contained in a net list file into a configuration bit pattern file.[1]

Thus, the numerous discussions of "converting" operations in *Butts et al.* are directed to the operation of a software tool, not any sort of integrated circuit operation of a device within the emulator system.

Accordingly, *Butts et al.* does not show "at least one circuit block manufactured to

[1] *Butts et al.*, Col. 9, Lines 40-43, emphasis added.

perform a predetermined data communication function including converting received first data values into second data values", as recited in claim 1. To show such a limitation, the rejection relies on the following portion of the reference.

> As per claim 1, Butts et al. disclose... a communication portion with at least one circuit block to perform conversion of data values (columns 76-78).[2]

A word search of the entire reference was performed to find all references to the words "communication" and all words starting with the letters "conver" (to cover conversion, convert, etc.). Such search found no reference or suggestion for a circuit block that provides the very particular data conversion function of claim 1.

In the portion of the reference cited by the rejection (columns 76-78), no reference could be found for such a circuit block. The following is believed to a fair representation of the teachings set forth in columns 76-78 of *Butts et al.*, and believed to demonstrate that the above excerpts do not show or suggest all limitations of claim 1.

Column 76 of *Butts et al.* describes a "Realizer Execution System" that acts a universal hardware device. Possible functions of such a system are a logic simulation hardware accelerator, a routing hardware accelerator, a hardware graphic processor, a real-time spectrum analyzer, or special effects synthesizer. There is no description of any particular circuit block, let alone one with the claimed data communication function as recited in claim 1.

Columns 76-77 describe a "Realizer Production System" that teaches how electrically re-programmable chips of an emulator can be substituted with programmable logic chips and corresponding PROMs to provide an actual hardware implementation of an emulated device. Again, there is no description of any particular circuit block, let alone one with the claimed data communication function.

Columns 77-78 describe a "Realizer Computing System" which teaches how the emulator can implement computing function specified by a high level computer language (as opposed to a netlist). This portion of reference does not describe any particular circuit block, let alone one with the claimed data communication function.

Thus, it is believed that the above presents clear rebuttal evidence that the portions of *Butt*

[2] See the Office Action, dated 5/23/03, Page 2, Section 1.

et al. relied upon in the rejection do not show Applicants' claim limitation of "at least one circuit block manufactured to perform a predetermined data communication function including converting received first data values into second data values".

If it is still believe that that above (or any other) portion of the reference shows such a claim limitation, Applicants respectfully request clarification of where and how such a teaching is found.

Accordingly, because the cited reference does not show or suggest all limitations of claim 1, this ground of rejection is traversed.

Various claims depending from claim 1 have additional limitations not shown in the cited reference.

Claim 4 adds that the integrated circuit also includes a timing circuit that receives a clock signal and generates an internal clock signal that is phase shifted with respect to the clock signal. Such a limitation is not shown in the cited reference *Butts et al.* The rejection relies on the following to show the limitations of claim 4.

> As per claim 4, Butts et al. disclose... a timing circuit that receives a clock signal and generates an internal clock signal (columns 67-69).[3]

In the portion of the reference cited by the rejection (columns 76-78), no reference could be found for such a received clock signal and phase shifted internal clock signal. The following is believed to a fair representation of the teachings set forth in columns 67-69 of *Butts et al.*, and demonstrates that the above excerpts do not show or suggest all limitations of claim 4.

Columns 67-68 include the word "clock" only once. The context is set forth below.

> Each timestep with events is mapped into one `sync clock` cycle of edge sensitive stimulators, instead of a vector memory location.[4]

Thus, all of columns 67-68 describe but <u>one</u> clock of a simulation system. Thus, this portion of the reference does not show both a clock signal and phase shifted internal clock signal, as recited

[3] See the Office Action, dated 5/23/03, Page 2, Section 1.
[4] *Butts et al.*, Col. 67, Lines 8-10.

in claim 4.

Column 69 describes how delay models can be introduced into an emulator. Column 69 describes a unit delay model that utilizes a continuous time clock. The time clock can be M times the frequency of a vector stimulus clock ECLK. However, neither clock is generated to be phase shifted with respect to the other, as recited in claim 4.

Thus, it is believed that the above presents clear rebuttal evidence that the portions of *Butt et al.* relied upon in the rejection do not show Applicants' claim 4 limitation of "an internal clock signal that is phase shifted with respect to the clock signal".

If it is still believe that that above (or any other) portion of the reference shows such a claim limitation, Applicants respectfully request clarification of where and how such a teaching is found.

Claim 7 recites that a data operation circuit includes a block converter circuit that converts input data words into output data words of different bit sizes. This limitation is not shown in the reference.

To show the limitations of claims 7, the rejection cites columns 45 and 46 of *Butts et al.* This rejection is not understood. Columns 45 and 46 describe software conversion functions, as noted with respect to claim 1. Thus, the "conversion" describes in the reference has nothing to do with data received by an integrated circuit, but rather data used to design a circuit emulator.

If it is still believe that that above (or any other) portion of the reference shows such a claim limitation, Applicants respectfully request clarification of where and how such a teaching is found.

Claims 8 and 10 recite that a data operation circuit includes a scrambler circuit that performs a scramble operation on received data.

To show the limitations of claims 8, the rejection cites columns 32 and 33 of *Butts et al.* This rejection is not understood. Applicants contend that columns 32 and 33 describe vector memory designs. Vector memories supply input signals to a circuit under emulation. Thus, such teachings cannot show a scrambling function as recited in claim 8.

If it is still believe that that above (or any other) portion of the reference shows such a claim limitation, Applicants respectfully request clarification of where and how such a teaching is found.

For all of these reasons this ground of rejection is traversed.

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The rejection of claims 15-20 will now be addressed.

The invention of claim 15 is directed to a semiconductor integrated circuit that includes a programmable logic device having a communication portion embedded therein, the communication portion including non-programmable circuits designed to provide a selectable data communication function.

To address this ground of rejection, Applicants incorporate by reference herein the comments set forth above for claim 15. Namely, that *Butts et al.* does not describe an embedded communication portion, let alone a portion providing a selectable data communication function, as recited in claim 15.

It is particularly emphasized that in rejecting claims 15-20, the rejection cites columns 32, 33, 76 and 77. However, as noted above, columns 32 and 33 describe vector memory designs, and thus cannot show selectable data communication functions. Columns 76 and 77 describe changing a reprogrammable emulator to production system, and provide no mention of any data communication function, let alone a selectable data communication function.

Accordingly, this ground of rejection is traversed.

Rejection of Claims 21-23 Under 35 U.S.C. §102(b) based on U.S. Patent No. 5,457,786 (*Roush*).

The invention of claim 21 is directed to a method that includes performing predetermined logic functions on a programmable logic portion of an integrated circuit. The method also includes performing serial data communication functions on a communication portion of the integrated circuit that includes circuit blocks that are not synthesized with programmable logic device configuration data.

That is, Applicants' claim 21 recites the step of performing serial data communication functions on a (non-synthesized) communication portion of an integrated circuit, where the integrated circuit also includes a programmable logic portion. Such a step is not shown in the cited reference.

Roush teaches a serial data interface. The reference teaches building such an interface with various programmable logic devices (PALs). However, none of the PALs includes a non-synthesized portion that performs a serial data communication function. All the PALs of *Roush*

are standard PAL integrated circuits without any particular "built-in" serial communication circuits.

In particular, if reference is made to FIGS. 2A and 2B, of *Roush*, the circuit shown includes one PAL, shown as item 25. The PAL is never described as including any non-synthesized serial communication circuit on the same integrated circuit (device). Similarly, FIGS. 3A and 3B show PALs 31, 32, 35, 36, and 37, while FIGS. 6A and 6B show PALs 61 and 66. Again, none of these PALs are ever described as including a non-synthesized serial communication circuit.

It is believed that the above presents clear rebuttal evidence that the cited reference *Roush* does not show Applicants' claim 21 limitations. If it is still believed that that above (or any other) portion of the reference shows such a claim limitation, Applicants respectfully request clarification of where and how such a teaching is found.

The claims depending from claim 21 include limitations that cannot be shown in the cited reference.

Claim 22 recites particular steps that include scrambling data according to a selected polynomial value. The reference *Roush* never mentions the word "polynomial". Accordingly, such a limitation cannot be shown in the reference.

Similarly, claim 23 recites a particular encoding function. The reference *Roush* does not include any words that begin with the letters "encod" (e.g., encode, encodes, encoder, or encoding, etc.). Thus, such a limitation cannot be shown in the reference.

For all of these reasons, this ground of rejection is traversed.

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Claims 7 and 8 have been amended, not in response to the cited art, but to more clearly define the invention.

The present claims 1-23 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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